SYS TEC
ELECTRONIC

DIPmodul 164

Hardware Manual

Edition January 2002

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Index of Figures and Tables

Preface

This manual describes only the functions of the DIPmodul 164. The controller C164 is not described herein. Additional controller- and board-level information and technical descriptions can be found in appropriate microcontroller Data Sheets/User's Manuals. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" in front of the signal name (i.e.: /RD). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal.

Declaration of the Electro Magnetic Conformity for the DIPmodul 164

The DIPmodul 164 (henceforth product) is designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Note:
PHYTEC products lacking protective enclosures are subject to damage by Electro Static Discharge (ESD) and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The DIPmodul 164 is one of a series of PHYTEC DIPmodules that can be fitted with different controllers and, hence, offers various functions and configurations. PHYTEC supports all common 8- and 16-bit controllers in two ways:

(1) as the basis for Rapid Development Kits in which user-designed hardware can be implemented on a wrap-field around the controller and

(2) as insert-ready, fully functional micro-, mini- and phyCORE modules, which can be embedded directly into the user's peripheral hardware, design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market.

1 Overview of the DIPmodul 164

The DIPmodul 164 is an universal microcontroller single board computer in DIP-40 dimensions (22.5 mm x 55.5 mm). It can be populated with the C164x microcontrollers of the Infineon C16x family in MQFP-80 packaging. Single row SMD pin header connectors in 2.54 mm pitch are used. Various port lines of the microcontroller are available to the target application board on these connectors (*refer to Figure 1*). This allows the DIPmodul 164 to be plugged into a target application like a "big chip". The board is fully equipped with the necessary connections and is ready for immediate use (*refer to Figure 2*).

Features of the DIPmodul 164 :

- microcontroller board in DIP-40 dimensions
  (22.5 mm x 55.5 mm) achieved through modern SMD technology
- improved interference safety achieved through multi-layer PCB technology
- controller signals and ports extend to standard-width (2.54 mm) pins aligning two sides of the module, enabling it to be plugged like a "big chip" into target applications
- single power supply +5 V= / 80 mA (typ.)
- 128 kByte Flash (up to 256 kByte Flash on-board)[1]
- on-board Flash programming using PHYTEC FlashTools
- no dedicated Flash programming voltage required through use of 5 V Flash devices
- 32 kByte SRAM on-board (up to 256 kByte SRAM)[1]
- 2 kByte serial EEPROM (up to 128 kByte)[1]
- on-chip Bootstrap loader
- serial interface to connect an external RS-232 transceiver
- on-chip Full CAN interface with on-board CAN transceiver
- on-chip Real-Time Clock

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[1] :   For more information about additional configurations call PHYTEC.

- 20 MHz CPU frequency, achieved through doubling the external quartz frequency
- supports power management

1.1 Block Diagram
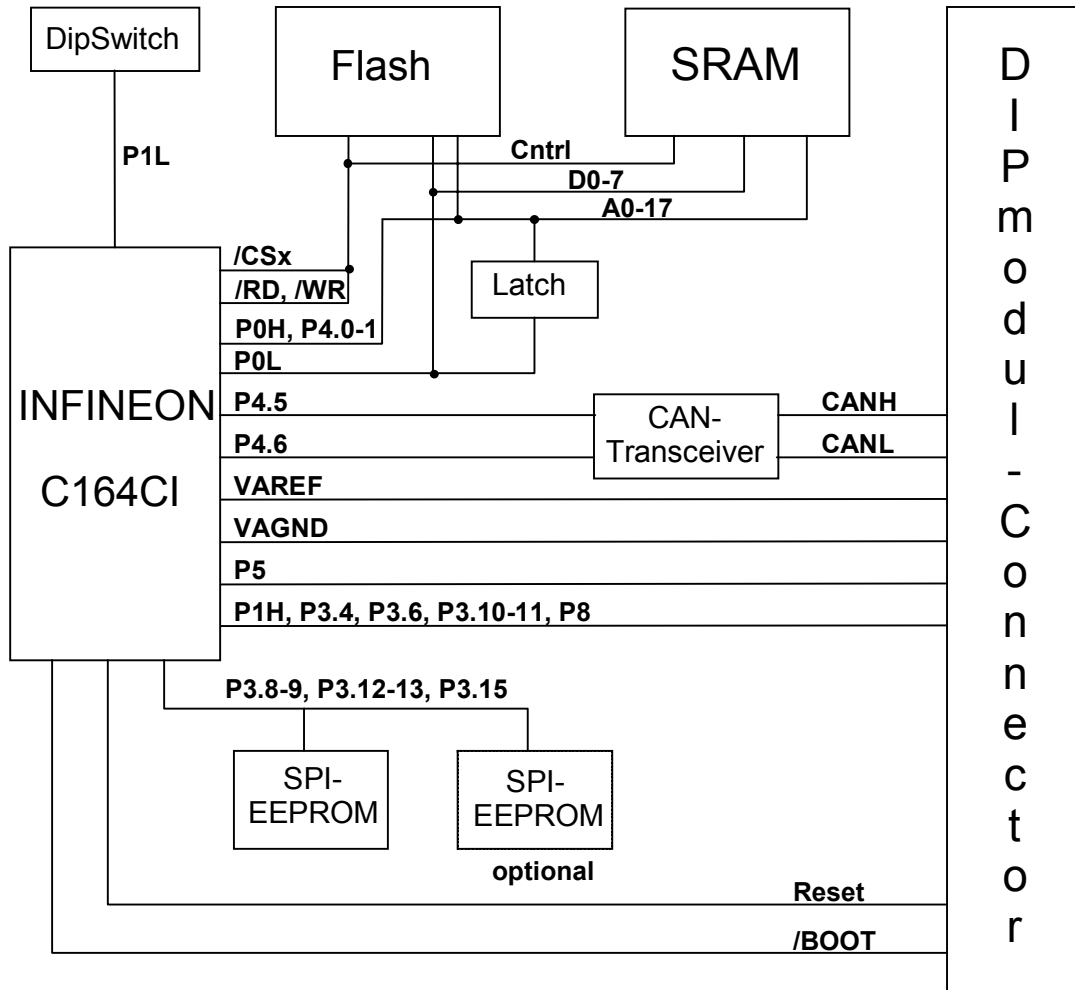
Figure 1:   Block Diagram

1.2 View of the DIPmodul 164
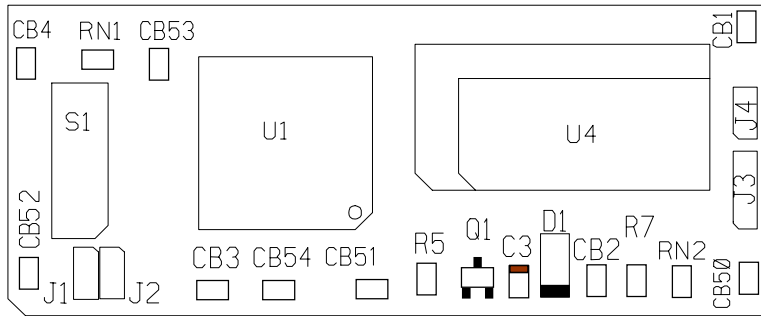
Figure 2:   View of the DIPmodul 164 (top view)
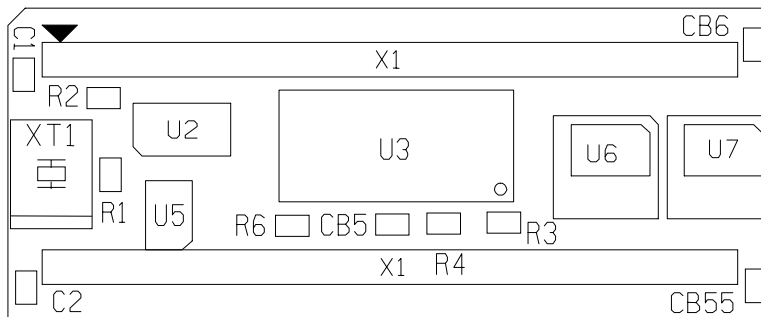
Figure 3:   View of the DIPmodul 164 (bottom view)

2 Pin Layout

Please note that all connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller's User's Manuals/Data Sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

As shown in *Figure 4*, all relevant signals are directed to the pin header connector X1 (referred to as DIPmodul-connector in this manual).

Many of the controller port pins accessible at the edges of the board have been assigned alternate functions that can be activated via software.

Table 1 shows an overview of the pinout of the DIPmodul-connector. For more information on alternative functions of the port pins, please see the User's Manual for the C164Cx.
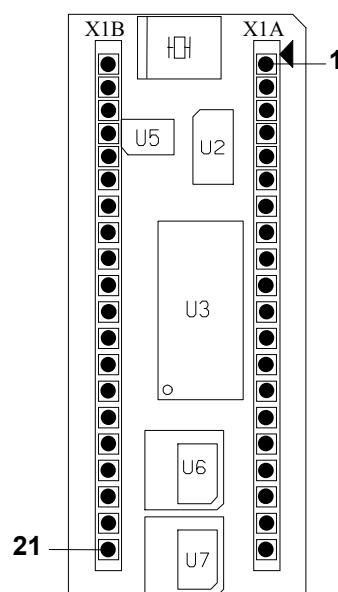
Figure 4:   Position of the Connectors (bottom view)

2.1 Pinout of the Pin Header Connector X1
(DIPmodul-connector)

Pin Number	Function	I/O	Description
Row X1A			
1	RxD0	I/O	Port pin P3.11 of the microcontroller
2	TxD0	I/O	Port pin P3.10 of the microcontroller
3	P3.4	I/O	Port pin P3.4 of the microcontroller
4	/BOOT	I	Boot signal input. Used to start the on-chip Bootstrap loader[1] of the C164. /BOOT = 0 during Reset 1-to-0 transition → start of the Bootstrap loader, enables serial Flash programming with PHYTEC FlashTools or communication with a monitor program
5	P36	I/O	Port pin P3.6 of the microcontroller
6, 7, 8	GND	-	Ground 0 V
9	VAREF	-	Reference voltage input of the on-chip A/D converter
10	VAGND	-	Analog Ground of the DIPmodul 164
11, 12, 13, 14, 15, 16, 17, 18	P5.0, P5.1, P5.2, P5.3, P5.4, P5.5, P5.6, P5.7	I	Port pins P5.0 – P5.7 of the microcontroller
19	RESIN	I	Reset input of the module, 0 - 1 transition triggers the RESET signal
20	GND	-	Ground 0 V
Row X1B			
21, 22	P8.0, P8.1	I/O	Port pin P8.0, P8.1 of the microcontroller
23, 24, 25, 26, 27, 28, 29, 30	P1H0, P1H1, P1H2, P1H3, P1H4, P1H5, P1H6, P1H7	I/O	Port pin P1H0 - P1H7 of the microcontroller (High Byte of Port 1)
31, 32	P8.2, P8.3	I/O	Port pin P8.2, P8.3 of the microcontroller
33, 34, 35	GND	-	Ground 0 V
36	P4.5 (RxDC)	I/O	Receive line of the on-chip CAN controller
37	CANL	I/O	CANL in-/output of the CAN transceiver
38	CANH	I/O	CANH in-/output of the CAN transceiver
39	P4.6 (TxDC)	I/O	Send line of the on-chip CAN controller
40	VCC	-	Power supply +5 V =

Table 1:   Pinout of the DIPmodul-connector

3 Jumper

For configuration purposes, the DIPmodul 164 has 4 solder jumpers, some of which have been installed prior to delivery. *Figure 5* illustrates the numbering of the jumper pads, while *Figure 6* indicates the location of the jumpers on the module. All solder jumpers (Jx) are located on the top side of the DIPmodul 164.
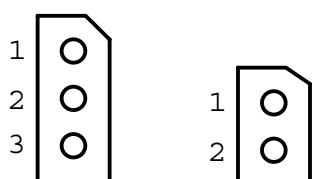
Figure 5:   Numbering of the Jumper Pads
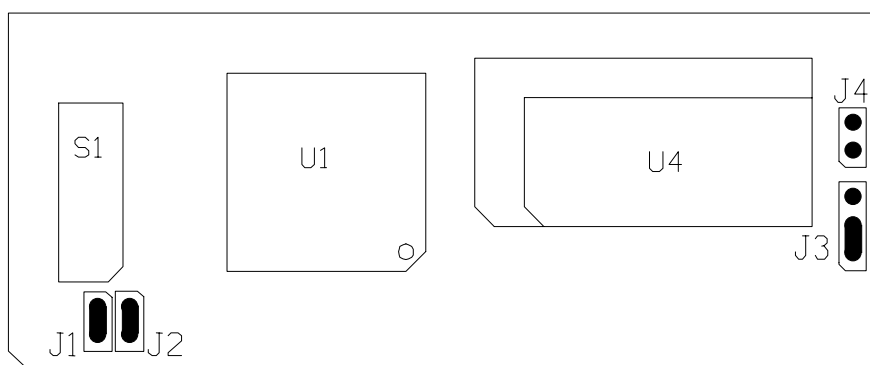
Figure 6:   Location of the Jumpers and Default Configuration (top view)

The jumpers (J = solder jumper) have the following functions:

	Default Configuration		**Alternative Configuration**	
J1, J2	(closed)	on-board CAN transceiver at P4.6 (TxDC) and P4.5 (RxDC)	(open)	Connection of an external CAN transceiver, as well as usage of ports P4.6 and P4.5 as digital in-/output is possible at pins X1B39 and X1B36
J3	(1+2)	RAM address line A17 connected to VCC; max. 128 kByte RAM memory at U4	(2+3)	RAM address A17 = microcontroller address A17; 256 kByte RAM at U4
J4	(open)	/NMI connected with a pull-up resistor. Activation of /NMI is not possible.	(closed)	/NMI connected with P8.3. Activation using a port pin or a modular connection is possible.

Table 2:   Jumper Settings Overview

3.1 J1, J2 CAN Interface

The CAN interface of the C164 is available at port P4.5 and P4.6. These signals extend to the CAN transceiver populating U5 (PCA82C251), which generates the signals CANH (Pin X1B38) and CANL (Pin X1B37). These signals can be directly connected to a dual-wire CAN bus. This requires that solder Jumpers J1 and J2 are closed.

Direct access to the signals RxDC/P4.5 and TxDC/P4.6 is also available on the DIPmodul-connector pins X1B36 and X1B39 if solder Jumpers J1 and J2 are open. This enables use of either an external CAN transceiver or use of P4.5 or P4.6 as standard I/O's.

Use of the on-chip CAN controller is possible only after the bit XPEN (SYSCON.2), found in the SYSCON register of the C164, is configured. For detailed descriptions of the CAN interface please refer to the appropriate controller User's Manual from Infineon, as well as corresponding publications for the CAN bus.

The following configurations are possible:

Use of the Port Pins P4.5 and P4.6	J1	J2
on-board CAN transceiver is used	closed*	closed*
external CAN transceiver or P4.5 and P4.6 as I/O (RxDC at X1B36, TxDC at X1B39)	open	open

*= Default setting

Table 3:   J1 and J2 Port Pins P4.5 and P4.6 / CAN Interface

3.2 J3 SRAM Memory Sizes

The SRAM, located at U4, uses a multi-shape format, which allows mounting of different SRAM devices. The function of pin 30 of the SRAM varies depending on the memory size. It can be configured with Jumper J3.

- **32 kByte SRAM Device:**

When the SRAM device is organized as 32 k x 8-bit, pin 30 (U4) is dedicated as a power supply pin and, must be connected to VCC, to enable access to the SRAM device.

- **128 kByte SRAM Device:**

When the SRAM device is organized as 128 k x 8-bit, pin 30 (U4) is defined as a high active Chip Select signal, and is must be connected to VCC, to enable access to the SRAM.

- **512 kByte SRAM Device:**

When the SRAM device is organized as 512 k x 8-bit, pin 30 (U4) is used as address line A17, and must be connected with address line A17 of the microcontroller. Only address lines A0 – A17 are used for memory access in the supported memory model. Consequently, the maximum useable memory size is 256 kByte. The address line A18 of the SRAM device is connected to GND.

In the default configuration, the DIPmodul 164 is populated with a 32 kByte SRAM memory located at U4[1].

Memory Size of U4	J3
32 kByte	1 + 2*
128 kByte	1 + 2
256 kByte	2 + 3

*= Default setting

Table 4:   J3 SRAM Memory Size Configuration

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[1] :   For more information about additional configurations see the PHYTEC Product Catalog.

3.3 J4 Activating /NMI

Jumper J4 activates the function of the /NMI on the microcontroller. Closing Jumper J4 allows control of the /NMI input via an external signal connected to pin X1B32 of the DIPmodul-connector (P8.3 inactive). Alternatively a software generated signal at port P8.3 can control the /NMI function. This function is required to activate the power-down mode of the controller. If Jumper J4 is open use of the /NMI is not possible.

/NMI	J4
Control of /NMI is not possible	open*
Control of /NMI possible	closed

*= Default setting

Table 5:   J4 Activating the /NMI
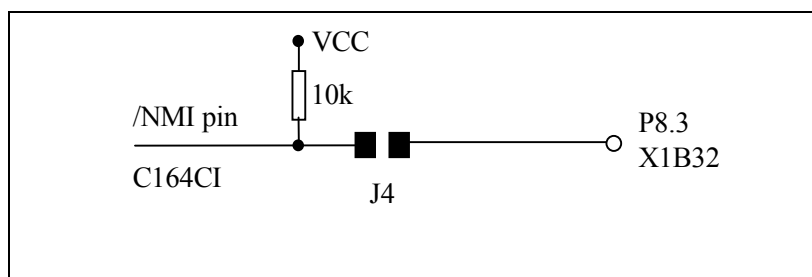
Figure 7:   Connection of the NMI Input to the DIPmodul 164

4 Configuration During System Reset

Although most of the programmable features of the C164 are either configured during the initialization phase or repeatedly during program execution, there are some features that must be configured earlier. These features are important for the first code fetch and, hence, the correct execution of the initialization routine as well. Of particular importance to the system startup configuration are the characteristics of the external bus interface, which supports the module's memory (for example data width, multiplexed or demultiplexed mode etc.).

These selections are made during reset via the pins of Port P0, which are read at the and of the internal reset sequence. During reset, internal pull-up devices are active on the Port P0 lines, so their input level is high, if the respective pin is left open. To change the configuration, external pull-down devices must be connected to the respective pin which generates a low level at the applicable input.

All of the configurations shown below are fixed and must not be changed. The following tables describe Port P0 and the function of the pins during system startup configuration.

Function of Port P0 during System Reset (High Byte)			
Bit H7 H6 H5	H4 H3	H2 H1	Bit H0
CLKCFG *1 0 1*	SALSEL *1 1*	CSSEL *1 1*	WRC 1
Double the external clock signal (f_{XTAL} * 2)	Support 256 kByte address space	Support /CS0 and /CS1[1]	/WR pin functions as /WR signal, function of P3.12 is configured by software

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[1] : If ports P4.0 to P4.3 are configured as segment addresses and chip select outputs, the segment address signal takes preference. I.e. although CSSEL is configured with 11 only 2 /CS signals are available.

Function of Port P0 during System Reset (Low Byte)			
Bit L7 L6	L5 L4 L3 L2	L1	Bit L0
BUSTYP *0* *1*	SMOD *1* *1* *1* *1*	ADP *1*	EMU *1*
8-bit multiplexed address and data bus	Execution of programs out of the external code memory is supported	Adapt Mode is not supported	Emulation Mode is not supported

Table 6:   System Startup Configuration after Reset

5 On-board Memory Configuration

The following section describes the configuration of on-board memory devices of the DIPmodul 164. Flash memory is provided at U3 for storage of program code. Internal RAM or external SRAM is available to store program data. The bus interface for Flash and SRAM is configured at time of delivery.

5.1 Address/Data Bus Configuration

The C164 controller is configured to support an 8-bit multiplexed address/data bus, address lines A0-A17 as well as the Chip Selects /CS0 and /CS1. The address lines A0-A7 are multiplexed with data lines D0-D7 and available at port P0L. The maximum address space per memory device (Flash, SRAM) is 256 kByte in this configuration.

Write access is obtained with the /WR[1] signal exclusively. The /CS0 (P4.3) signal controls access to the Flash memory while /CS1 (P4.2) activates the SRAM device.

This DIPmodul 164 is offered with various memory configurations. The corresponding values must be entered in the startup code for the C164 controller in order to properly select the address space and access control.

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[1] : The port pin 3.12 must not be configured as BHE since this pin controls access to the on-board EEPROM.

5.2 Flash Memory (U3)

Flash, as non-volatile memory on the DIPmodul 164, provides an easily reprogrammable means of code storage to the user. The DIPmodul 164 can be populated at U3 by a single Flash device of type 29F010 with two banks of 64 kByte each or device type 29F040 with 8 banks of 64 kByte each. When mounted with a 29F040 type Flash, only 256 kByte of the 512 kByte can be accessed by the controller (*refer to section 4*). Flash memory devices offer up to 100,000 reprogramming cycles, and enable on-board programming of user code. These Flash devices are programmable with 5 V. No dedicated programming voltage is required. Access to the Flash memory is controlled by /CS0.

Type	Size	Manu-facturer	Device Code	Man. Code	Access Time[1]	MCTCO[2]
29F010	128 kByte	AMD	20h	01	90 ns	14
29F002NBT	256 kByte	AMD	B0h	01	90 ns	14
29F002NBB	256 kByte	AMD	34h	01	90 ns	14
29F040	512 kByte	Fujitsu	A4h	04	90 ns	14
29F040	512 kByte	AMD	A4h	01	90 ns	14

Table 7:   Flash Memory

A value of MCTC0 = 14 configures one wait state (number of wait states = 15 - MCTC0).

All standard versions of the DIPmodul 164 feature a programming utility – FlashTools (*refer to applicable QuickStart Instruction for more details*) – that allows for convenient on-board programming.

Use of a Flash device as the only code memory results in limited usability of the Flash as non-volatile memory for data. This is due to the internal structure of the Flash device as, during the Flash's internal programming process, the reading of data from Flash is not possible. For Flash programming, program execution must be transferred out of Flash (such as into von Neumann RAM). This usually equals the interruption of a "normal" program execution cycle.

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[1] : Contact SYSTEC/PHYTEC for more information about additional configurations.
[2] : MCTC0 – Memory Cycle Time in BUSCON0 register,
     number of wait states = [15 - MCTC]

As of the printing of this manual, Flash devices generally have a life expectancy of at least 100,000 erase/program cycles.

5.3 SRAM Memory (U4)

Access to the SRAM memory is controlled by /CS1 and achieved using an 8-bit data bus. The SRAM, located at U4, uses a multi-shape format, which allows mounting of different SRAM devices. The function of pin 30 of the SRAM varies depending on the memory size. It can be configured with Jumper J3 (*refer to section 3.2 for more details*).

- **32 kByte SRAM Device:**
When the SRAM device is organized as 32 k x 8-bit, pin 30 (U4) is dedicated as a power supply pin and, must be connected to VCC, to enable access to the SRAM device.

- **128 kByte SRAM Device:**
When the SRAM device is organized as 128 k x 8-bit, pin 30 (U4) is defined as a high active Chip Select signal, and is must be connected to VCC, to enable access to the SRAM.

- **512 kByte SRAM Device:**
When the SRAM device is organized as 512 k x 8-bit, pin 30 (U4) is used as address line A17, and must be connected with address line A17 of the microcontroller. Only address lines A0 – A17 are used for memory access in the supported memory model. Consequently, the maximum useable memory size is 256 kByte. The address line A18 of the SRAM device is connected to GND.

In the default configuration, a 32 kByte SRAM device with 90 ns access time populates the DIPmodul 164 at U4[1]. The value of bit MCTC1 (located in the BUSCON1 register) must be set to 14 if the access time is 90 ns.

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[1] : For more information about additional configurations see the PHYTEC Product Catalog or contact PHYTEC.

6 Memory Models

The following sections provide examples for the configuration of two memory models of the DIPmodul 164. Please note, that the /CS0 (P4.3) signal controls access to the Flash memory while /CS1 (P4.2) activates the SRAM device. Other /CS signals are not configured. The C164 controller is configured to support an 8-bit multiplexed address/data bus. The maximum address space per memory device (Flash, SRAM) is 256 kByte in this configuration. Write access to both SRAM and Flash is obtained with the /WR[1] signal exclusively.

This DIPmodul 164 is offered with various memory configurations. The corresponding values must be entered in the startup code for the C164 controller in order to properly select the address space and access control.

6.1 Runtime Model

The microcontroller always begins with a command execution (Reset inactive, no Bootstrap mode) at address 0 with active /CS0. Code access is therefore directed to Flash memory (U3). The Flash memory must contain the user application at address 0. Access to the SRAM (U4) is possible only after initialization of the /CS1 signal in regards to size, address range and access mode. Normally, this memory model is used for start-up of the user application out of the Flash, and is therefore called runtime model.

In the runtime model, the SRAM should be configured to start after the Flash memory range in the address space of the microcontroller. Since the Flash is available at 0x00000, and has a capacity up to 256 kByte, it is recommended that the SRAM start address is 0x40000. The size of the SRAM memory range can be configured by software according to the available memory size.

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[1] : The port pin 3.12 must not be configured as BHE since this pin controls access to the on-board EEPROM.

When using the Flash memory in an application, please note that the address space from 0x00E000 – 0x00FFFF is reserved for access to the internal XRAM/CAN and RAM/SFR areas. This address range must be reserved while linking an application.

6.2 Programming Model

Using the Bootstrap mode of the C164 the microcontroller is able to receive and execute program code via the serial interface. In this mode it is also possible to configure the start address and the size of the on-board SRAM (U4) connected to /CS1, enabling access to the SRAM at address 0. This feature is used for the execution of FlashTools, as well as the monitor program. This memory model is known as the programming model.

In the programming model, the SRAM should be configured to start before the Flash memory range in the address space of the microcontroller. If the monitor program is used in support of the debugger, it is advised that the differences between the position of the address space for the program code and the program data are minimal. We recommend to configure the SRAM in the address space from 0x00000 – 0x03FFFF for storage of program code and in the address space from 0x40000 – 0xFFFF for storage of program data. Since only one physical SRAM device is used, the SRAM should be divided into two areas and used by the applications separately as program code and program data.

7 On-Board Peripherals

The following sections describe the on-board peripherals of the DIPmodul 164. Further information on the peripherals of the microcontroller can be found in the hardware manual of the C164.

7.1 Clock Generation

A 10 MHz quartz populates the DIPmodul 164. With the choosen configuration for the PLL of the microcontroller (*refer to section 4*), the frequency of the quartz is doubled. The CPU then operates at a 20 MHz frequency (default configuration).

7.2 Reset

A capacitor of 4,7 μF is connected to the reset input of the microcontroller. This enables releasing an automatic reset during power-on. During power-on, the capacitor is charged via a resistor 50°kOhm – 150°kOhm in size. This results in a low-level at the reset input of the microcontroller for approximately 40 ms – 120 ms.
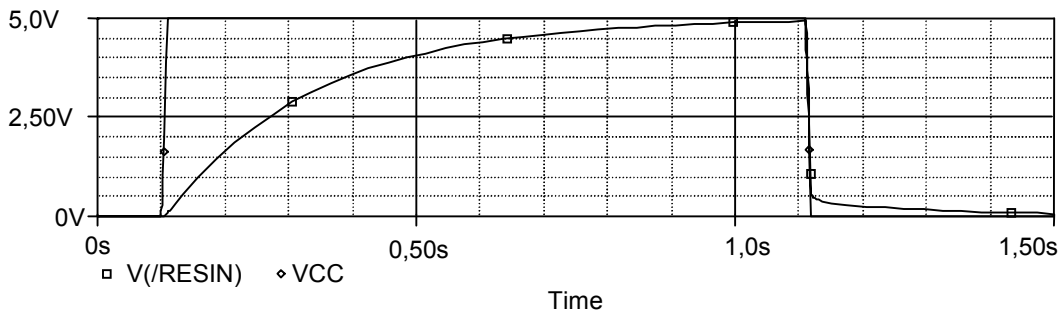

Figure 8:   *Timing Diagram at /RESIN (C164CI) during Power-on and Power-off (R=50 k, C3=4700 nF)*

Alternatively it is possible to reset the DIPmodule-164 manually via pin X1A19 of the DIPmodul-connector. This is necessary when the supply voltage increases slowly, and therefore the automatic reset will not work.

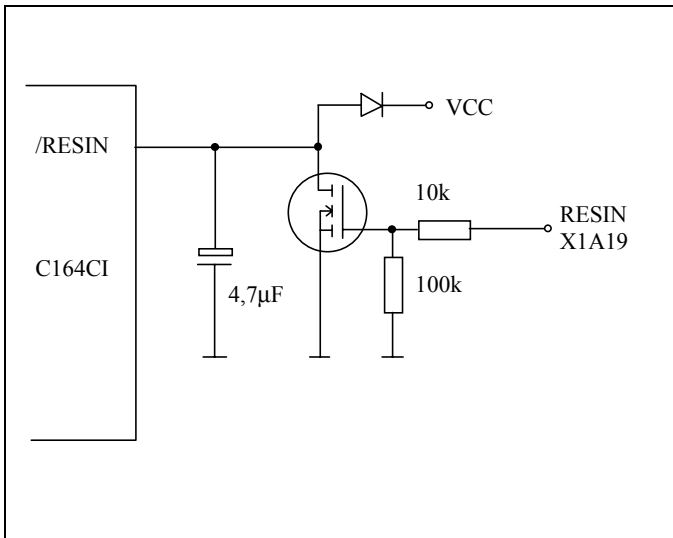*Figure 9:   Circuitry of the Reset Input on the DIPmodul 164*

7.3 /BOOT

The C164 has a built-in Bootstrap loader that supports loading and execution of user programs using the serial interface. The Bootstrap loader starts if the Boot input is connected to GND via a pull-down resistor during a high-to-low transition of the RESIN signal.
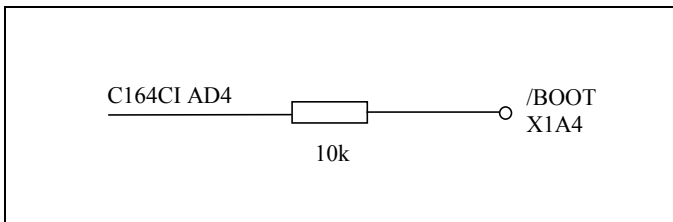

Figure 10:   Circuitry of the Boot Pin on the DIPmodul 164

7.4 DIP-Switch S1

The on-board DIP switch S1 is connected with port P1L. The following table describes the switch position and the resulting signal level on the port pins.

Switch	Switch Position	Port Pin Level
S1.1	OFF	P1L.0 = 1
	ON	P1L.0 = 0
S1.2	OFF	P1L.1 = 1
	ON	P1L.1 = 0
S1.3	OFF	P1L.2 = 1
	ON	P1L.2 = 0
S1.4	OFF	P1L.3 = 1
	ON	P1L.3 = 0
S1.5	OFF	P1L.4 = 1
	ON	P1L.4 = 0
S1.6	OFF	P1L.5 = 1
	ON	P1L.5 = 0
S1.7	OFF	P1L.6 = 1
	ON	P1L.6 = 0
S1.8	OFF	P1L.7 = 1
	ON	P1L.7 = 0

Table 8:   Connection of DIP-Switch S1 to Port P1L

7.5 Serial Interfaces

The microcontroller features an on-chip UART. The RxD0 (X1A1, P3.11) and TxD0 (X1A2, P3.10) pins of DIPmodul-connector can be used to connect to an external RS-232 or RS-485 transceiver.

The RxD0 and TxD0 pins on the DIPmodul 164 provide TTL levels, and therefore must not be connected to RS-232 signals. An external transceiver is required for connection to an RS-232 interface.

7.6 CAN Interface

The DIPmodul 164 is equipped with a C164CI controller. One of the special features of this controller is the on-chip Full-CAN controller which enables the integration of the DIPmodul 164 in a CAN network. Running the C164CI controller with 20 MHz CPU clock, a CAN bit rate of up to 1 MBit/s can be achieved.

Bit Rate	BTR0	BTR1
10 kBit/s	71h	2Fh
50 kBit/s	49h	2Fh
125 kBit/s	44h	1Ch
250 kBit/s	41h	2Fh
500 kBit/s	41h	16h
1000 kBit/s	40h	16h

Table 9:   Selected Bit Rates with 20 MHz CPU Frequency

The bit rates in *Table 9* are only examples. For specific applications, the values for sample point and the synchronization jump width must be configured by the user.

The programming of the CAN controller is done by means of control registers which are mapped into the regular memory space of the controller in the address range 0x0EF00h through 0x0EFFFh. The exact meaning of the registers and description of how to program the controller can be found in the C164CI controller manual. When utilizing the CAN interface port pins P4.5 (RXDC) and P4.6 (TXDC) must be connected to the on-board CAN transceiver (U5) via jumpers J1 and J2. Using the CANH (X1B38) and CANL (X1B37) pins, it is possible to connect the module directly to a CAN bus. This requires that the difference in the signal potential between the connected CAN nodes stays below the limiting values specified for the CAN transceiver.

In CAN applications with significant differences on the signal levels on the connected CAN nodes it is recommended to use an optically isolated CAN transceiver. The CAN transceiver is then supplied by a voltage from the CAN bus that is common to all nodes. In order to

connect an optically isolated transceiver, Jumpers J1 and J2 must be opened. This enables connection of the TxDC (X1B39) and RxDC (X1B36) signals to an external CAN transceiver.

7.7 Serial EEPROM

The EEPROM (U6, U7) is intended for storage of non-volatile data during the runtime of an application.

In order to achieve the fastest, simplest possible method for communication to the EEPROM, the internal *"High Speed Synchronous Serial Interface"* (SSC) of the C164CI is used. The interface supports transmission according to the SPI standard.

EEPROM Signal	Connection C164	Description
/CS	U6: P3.12 U7: P3.15	In order to avoid access conflicts only one of the /CS lines selecting the EEPROM device can be active (low signal).
SO	P3.8	Serial data output
/WP	GND	Use of the Write Protect Enable Bits (WPEN) of the EEPROMs is supported.
SI	P3.9	Serial data input
SCK	P3.13	Clock input
/HOLD	VCC	Hold function is not supported. The SSC interface supports the transmission of continuous data streams.

Table 10:   Connecting the EEPROM

Depending on the EEPROM used, a transmission rate of up to 5 MBaud can be achieved. *Table 11* gives an overview of EEPROM types and manufacturers.

Size	Device	Manufacturer	Max. Baud Rate
2 kByte	AT25160	ATMEL	2 MHz
2 kByte	X25170	XICOR	5 MHz
2 kByte	25C160	Microchip	3 MHz
8 kByte	AT25640	ATMEL	2 MHz
8 kByte	X25650	XICOR	5 MHz
16 kByte	AT25128	ATMEL	3 MHz
32 kByte	AT25256	ATMEL	3 MHz
64 kByte	AT25H512	ATMEL	5 MHz

Table 11:   Selected Serial EEPROMs (Manufacturers, Baud Rates)

In order to store larger data quantities, it is possible to populate the board with up to two serial EEPROMs. This expands memory capacity up to 128 kByte (data valid as of printing of this manual). This enables a complete copy of the recent data to be kept during runtime of an application. In case of power failure, data is preserved, the application can reload data from the EEPROM and continue code execution at the point where it was interrupted.

8 Technical Specifications

The physical dimensions of the DIPmodul 164 are represented in *Figure 11*. The module's profile is about 12 mm thick, with a maximum component height of 3 mm on the pin-side of the PCB and approximately 4 mm on the CPU-side. The board itself is approximately 1,6 mm thick.
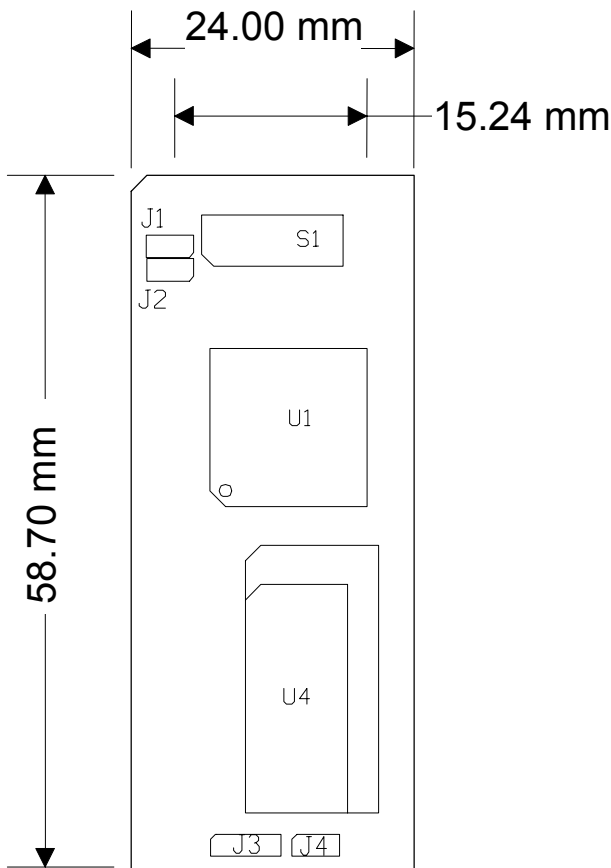

Figure 11:   Physical Dimensions (not shown at scale)

The data represent the standard configuration of the DIPmodul 164 as of the printing of this manual.

Additional specifications:

Electrical Parameters

- Operating voltage: 5 V ± 10 %
- Power consumption: typ. 80 mA, 128 kByte Flash, 32 kByte SRAM, 2 kByte EEPROM,
  CAN transceiver, 20 MHz CPU frequency, 25°C
- Clock generation   20 MHz CPU frequency, achieved by doubling the external quartz frequency (10 MHz)

Environment Conditions

- Operating temperature: Standard: 0°C to + 70°C
  Extended: - 40°C to + 85°C
- Storage temperature: - 40°C to + 90°C
- Humidity: max. 90 % not condensed

Mechanical Specifications

- Size: 24.0 mm x 58.7 mm ± 0.3 mm
- Weight: approximately 10.5 g
- Pin header receptacles: 40-pin dual inline IC socket, standard width 2.54 mm
- Pin header rows: standard width 2,54 mm, Ø 0,47 mm; contact length 3.2 mm

These specifications describe the standard configuration of the DIPmodul 164 as of the printing of this manual.

9 Hints for Handling the Module

Removal of individual components on the DIPmodul 164 (controller, memory, standard quartz etc.) is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board, as well as surrounding components and sockets, remain undamaged while desoldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

When changing the controller ensure that the controller to be used is pin-compatible to the C164 Controller and that special hardware features are compatible with the layout of the board.

Appendix A

Hints for Using PHYTEC FlashTools 16W

When using FlashTools 16W for on-board download of application program on the DIPmodul 164, the following must be considered:

Note:
Due to an error in FlashTools both the *Flash Information* and the *Sector Utilities* window will show twice as many sectors as physically available on the DIPmodul 164. This must be considered when erasing or writing to the corresponding Flash sectors. Any attempt erasing or writing to the upper mirrored sectors will cause an error. Furthermore, the values show in the *Protection* field are wrong and do not reflect the actual protection state. This error will be resolved in a new version of FlashTools.

Always use the lower 4 Flash sectors on a DIPmodul 164 in conjunction with PHYTEC FlashTools 16W.

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