SYS TEC ELECTRONIC

Development Board ECUcore-9G20

Hardware Manual

Edition March 2010

Status / Changes

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Date/ Version	Section	Change	Editor
L-1256e_01		initial version	K.Becker

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	WORLDWIDE
Address:	SYS TEC electronic GmbH August-Bebel-Str. 29 D-07973 Greiz GERMANY
Ordering Information:	+49 (3661) 6279-0 info@systec-electronic.com
Technical Support:	+49 (3661) 6279-0 support@systec-electronic.com
Fax:	+49 (3661) 62 79 99
Web Site:	http://www.systec-electronic.com

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1 Introduction

The ECUcore-9G20 Development Board provides a flexible development platform, enabling quick and easy start-up and subsequent programming of the Single Board Computer module. The design of the Development Board allows easy operation of the installed ECUcore in **C**ommunication **N**etworks (LAN, USB, CAN) and simple GPIO-Tests by keys and leds. Components for SPI and I²C enable easy testing of these bus-systems. A connection of additional expansion board features for various functions is supported, to allow fast and convenient prototyping and software evaluation.

For the SYS TEC IEC 61131-3 PLC firmware, an additional RUN/STOP/MRES switch is provided on the Development Board as well as one RUN LED and one ERROR LED for indicating the operating mode of the IEC 61131-3 PLC.

This manual describes the functionality of the Development Board. Precise specifications of the installed ECUcore or the controller that is implemented on the ECUcore can be found in the applicable Hardware Manual or the User's Manual and Data Sheet of the controller. The functions or descriptions of the ECUcore and the microcontroller are not included in this Hardware Manual! These documentations are not relevant for the basic functionality of the Development Board.
Please refer to the corresponding manuals and documentations for any other board components you may use (USB host, Ethernet switch, etc.).

Low-active signals are denoted by a „/“ in front of the signal name (i.e. “/RD”). The representation “0” indicates a logical-zero or low-level signal. A “1” is the synonym for a logical one or high-level signal.

2 Ordering Information and Support

Order Number	Version
4002008	Development Board ECUcore-9G20

Development Board features:

- Socket for ECUcore-9G20 (order number: 4001016)
- External power supply from 9-36VDC/24W
- Switching regulator 9-36VDC / 5VDC
- Switching regulator 9-36VDC / 3,3VDC
- 4 keys and 4 led's free usable for development
- 1 8-position dip-switch
- 1 3-position slider switch and 2 leds for using with PLC firmware
- Boot and reset key plus reset and shutdown led
- Battery for buffering Real time clock on ECUcore
- EEPROM 16kiB as SPI example
- Potentiometer as analog input
- microSD-card socket
- 1 USB device connector for onboard USB device on ECUcore
- 2 USB2.0 host conectors for onboard USB host on ECUcore
- 1 Ethernet connector for onboard PHY on ECUcore
- 1 CAN interface with D-Sub 9 connector
- 3 RS232 interfaces with 2 D-Sub 9 and 1 multi-pin connector
- 20pin ICE/JTAG interface for Atmel 9G20 microcontroller
- 10pin JTAG interface for FPGA
- All freely usable pins of the ECUcore are brought out to an expansion connector, 2x 120pol pin contact stripes with user-friendly 2,54mm contact spacing

3 Properties of the Development Board

3.1 Overview

The ECUcore-9G20 belongs to SYS TEC's ECUcore family. The ECUcore-9G20 integrates all elements of a microcontroller system on one board. The module only needs an external power supply (3,3V) to operate. The Development Board was build for accessing all interfaces of the ECUcore and rapid development of software drivers and applications. Some special drivers or external controllers are helpful to interact with the environment (bus-systems and control elements). All interfaces are brought out on standard connectors (RJ45, D-SUB).

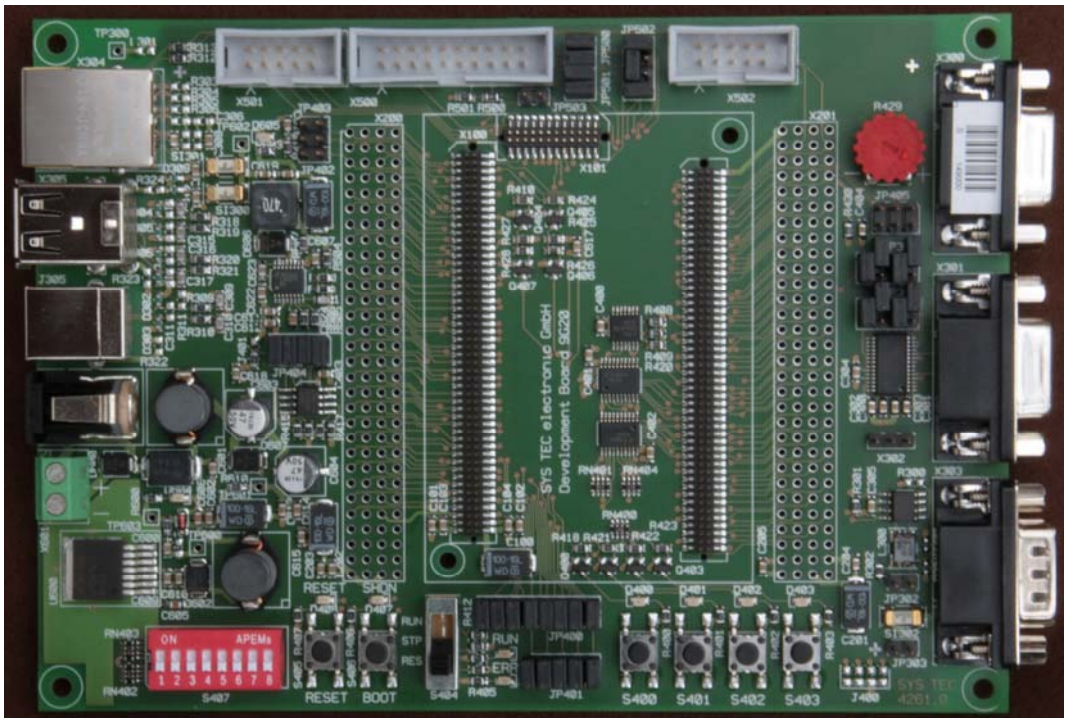


Figure 1: Development Board ECUcore-9G20

The dimensions of the board are 160mm x 115mm.

3.2 Block Diagram

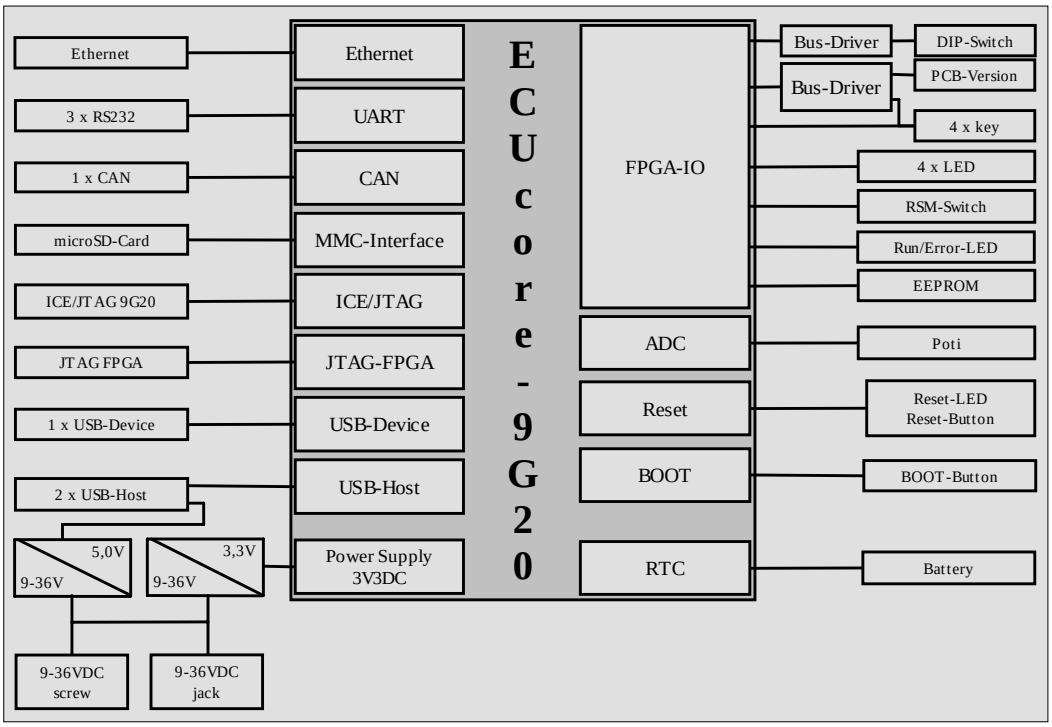


Figure 2: Block Diagram Development Board ECUcore-9G20

3.3 Positions of Elements

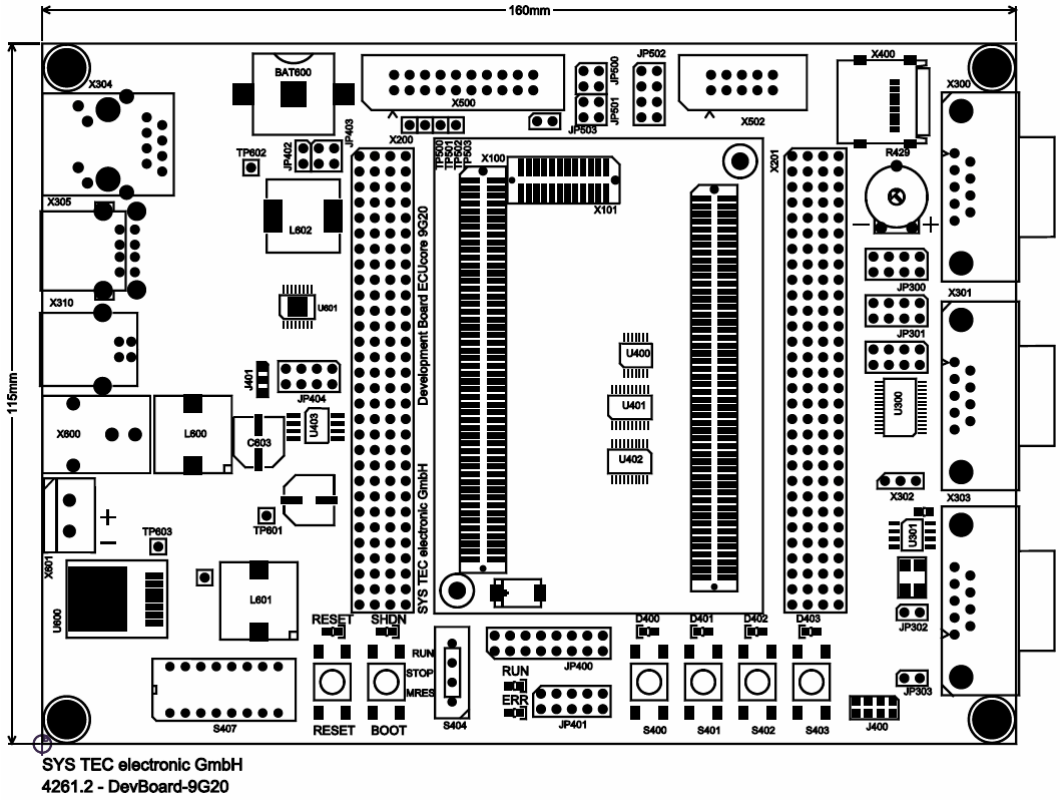


Figure 3: Positions of components

3.4 Jumper

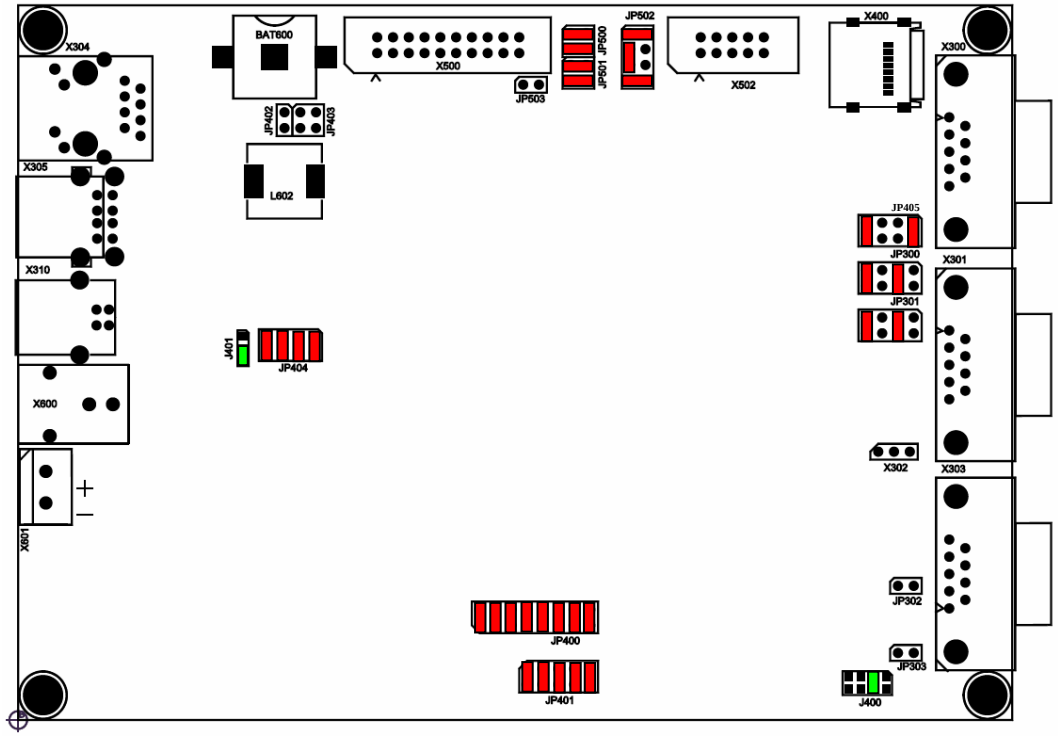


Figure 4: Default Jumper configuration

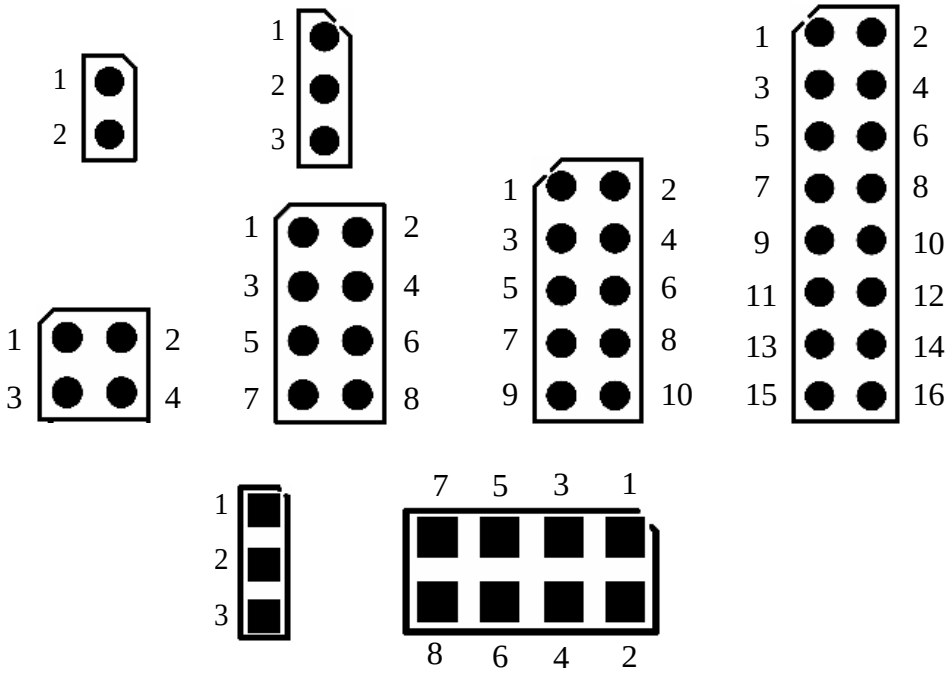


Figure 5: Jumper pincount

Jumper	Signal	Jumper Setting (closed)	Function
JP300	TXD1, TXD0 DTXD, TXD2	1-2	Signal TXD2 is on X302
		3-4 default	Signal DTXD is on X301
		5-6	Signal TXD0 is on X300
		7-8 default	Signal TXD1 is on X300
JP301	RXD1, RXD0 DRXD, RXD2	1-2	Signal RXD2 is on X302
		3-4 default	Signal DRXD is on X301
		5-6	Signal RXD0 is on X300
		7-8 default	Signal RXD1 is on X300
JP302	CAN-Termination	1-2	Termination 120R on CAN active
JP303	CAN-VCC	1-2	CAN-VCC (5,0VDC) is on Pin 1 of X303 present (Fuse with 125mA)
JP400	FPGA_IO_69 FPGA_IO_70 FPGA_IO_71 FPGA_IO_72 FPGA_IO_73 FPGA_IO_74 FPGA_IO_75 FPGA_IO_76	1-2 default	LED D400 is on FPGA_IO_69
		3-4 default	LED D401 is on FPGA_IO_70
		5-6 default	LED D402 is on FPGA_IO_71
		7-8 default	LED D403 is on FPGA_IO_72
		9-10 default	Button S400 is on FPGA_IO_73
		11-12 default	Button S401 is on FPGA_IO_74
		13-14 default	Button S402 is on FPGA_IO_75
		15-16 default	Button S403 is on FPGA_IO_76
JP401	FPGA_IO_77 FPGA_IO_78 FPGA_IO_79 FPGA_IO_80 FPGA_IO_81	1-2 default	LED D405 is on FPGA_IO_77
		3-4 default	LED D406 is on FPGA_IO_78
		5-6 default	Switch Status MRES is on FPGA_IO_79

Jumper	Signal	Jumper Setting (closed)	Function
		7-8 default	Switch Status Stop is on FPGA_IO_80
		9-10 default	Switch Status Run is on FPGA_IO_81
JP402	BMS	1-2	Signal BMS is set to 1 (high)
JP403	/BOOT WKUP	1-2	Signal /BOOT is set to 0 (low)
		3-4	Signal WKUP is set to 0 (low)
JP404	FPGA_IO_44 FPGA_IO_47 FPGA_IO_48 FPGA_IO_49	1-2 default	EEPROM Signal SPI-CLK is on FPGA_IO_49
		3-4 default	EEPROM Signal SPI-DI is on FPGA_IO_48
		5-6 default	EEPROM Signal SPI-DO is on FPGA_IO_47
		7-8 default	EEPROM Signal SPI-/CS is on FPGA_IO_44
JP405	AD0 AD1 AD2	1-2 default	Signal SD_SLOT (Open/close) is present on AD2
		3-4	Potentiometer R429 is present on AD2
		5-6	Potentiometer R429 is present on AD1
		7-8 default	Potentiometer R429 is present on AD0
JP500	ARM_TCK FPGA_TCK	1-2 default	JTAG-Signal FPGA_TCK is present on Pin 1 of X502
		3-4 default	JTAG-Signal ARM_TCK is present on Pin 1 of X502
JP501	ARM_TMS FPGA_TMS	1-2 default	JTAG-Signal FPGA_TMS is present on Pin 3 of X502
		3-4 default	JTAG-Signal ARM_TMS is present on Pin 3 of X502
JP502	ARM_TDO FPGA_TDO ARM_TDI FPGA_TDI	1-2 default	JTAG-Signal FPGA_TDI is present on Pin 7 of X502
		3-4	JTAG-Signal ARM_TDI is present on Pin 7 of X502
		5-6	JTAG-Signal FPGA_TDO is present on Pin 5 of X502
		7-8 default	JTAG-Signal ARM_TDO is present on Pin 7 of X502
JP503	/JTAGSEL	1-2	Signal /JTAGSEL is set to 1 (high) Boundary Scan Mode
J400	PCB-Version	1-2	Bit0 of Version on EBI D8
		3-4 default	Bit1 of Version on EBI D9
		5-6	Bit2 of Version on EBI D10
		7-8	Bit3 of Version on EBI D11
J401	EEPROM Write Protect	1-2	Write Protect of EEPROM is active
		2-3 default	Write Protect of EEPROM is not active

3.5 Board Connectors

See figure 3 for the position of board connetor X100 and its connector rows.

The Development Board ECUcore-9G20 has two board connectors. Each of the SMT male header consists of 100 contacts divided into double rows. In total, the board has 200 contacts. For better emc-properties, 20% of pins are GND.
A third connector at the front side is for connecting debug interfaces of the CPU, Power sequencer and FPGA. It is not mounted by default.

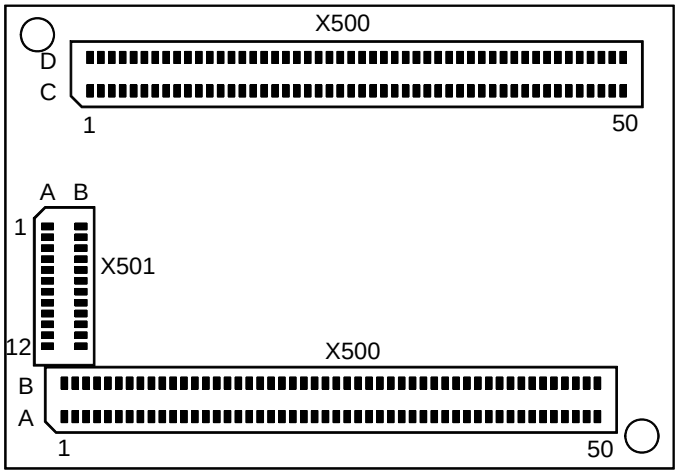


Figure 6: Pinout (top view)

The board connectors are equipped with the common and durable 1,27mm pitch. The type of the male header used on the Development Board is the '7072'-series provided by "W+P PRODUCTS".

Please refer to the datasheet and the electrical specifications.

Connectors:
ECUcore-9G20:

- W+P 6060-100-36-00-00-00-PPST (2x50pol. female)
- W+P 6060-024-36-00-00-00-PPST (2x12pol. female)

Development Board:

- W+P 7072-100-10-00-10-PPST (2x50pol. male)

- W+P 7072-024-10-00-10-PPST (2x12pol. male)

The following table defines the pinout.

Signal	Pin	Pin	Signal		Signal	Pin	Pin	Signal
GND	A01	B01	GND		GND	C01	D01	+2V5_EPHY
/BOOT	A02	B02	/MR		ETH0_TX-	C02	D02	GND
WKUP	A03	B03	/RESET		ETH0_TX+	C03	D03	ETH_SPEED
SHDN	A04	B04	/PFI		ETH0_RX+	C04	D04	ETH_LINK/ACT
BMS	A05	B05	WDI		ETH0_RX-	C05	D05	GND
GND	A06	B06	PS_IO		GND	C06	D06	AD0
DRXD	A07	B07	GND		ADTRG	C07	D07	AD1
DTXD	A08	B08	RTS0		ADVREF	C08	D08	AD2
DSR0	A09	B09	CTS0		GND	C09	D09	GND
DTR0	A10	B10	RTS1		SD_MCDA0	C10	D10	SD_MCDB0
DCD0	A11	B11	CTS1		SD_MCDA1	C11	D11	SD_MCDB1
GND	A12	B12	GND		SD_MCDA2	C12	D12	SD_MCDB2
TXD0	A13	B13	TXD1		SD_MCDA3	C13	D13	SD_MCDB3
RXD0	A14	B14	RXD1		SD_MCCK	C14	D14	SD_MCCDA
TXD2	A15	B15	TXD3		GND	C15	D15	SD_MCCDB
RXD2	A16	B16	RXD3		SCK0	C16	D16	GND
GND	A17	B17	TXD5		SCK1	C17	D17	TIOA1
USB_HDPA	A18	B18	RXD5		SCK2	C18	D18	TIOB1
USB_HDMA	A19	B19	GND		PCK1	C19	D19	TIOA2
USB_HDPB	A20	B20	USB_DDP		RK0	C20	D20	TIOB2
USB_HDMB	A21	B21	USB_DDM		TK0	C21	D21	TD0
GND	A22	B22	GND		RF0	C22	D22	RD0
I2C_DATA	A23	B23	CAN_TXD		TF0	C23	D23	GND
I2C_CLK	A24	B24	CAN_RXD		GND	C24	D24	FPGA_IO0
GND	A25	B25	CAN_VCC		FPGA_IO1	C25	D25	FPGA_IO2
FPGA_IO44	A26	B26	GND		FPGA_IO3	C26	D26	FPGA_IO4
FPGA_IO46	A27	B27	FPGA_IO45		FPGA_IO5	C27	D27	FPGA_IO6
FPGA_IO48	A28	B28	FPGA_IO47		FPGA_IO7	C28	D28	GND
FPGA_IO50	A29	B29	FPGA_IO49		GND	C29	D29	FPGA_IO8
FPGA_IO52	A30	B30	FPGA_IO51		FPGA_IO9	C30	D30	FPGA_IO10

Table 1: Pinout high density connectors

Most Signals are brought out of expansion connectors X200 and X201. These are pin contact stripes with standard 2,54mm contact spacing. So you can easily connect extensions for fast development.

X200	A	B	C	D
1	/BOOT	GND	/MR	GND
2	WKUP	/RESET	/SHDN	/PFI
3	BMS	GND	WDI	GND
4	PS_IO	DRXD	DTXD	RTS0
5	DSR0	GND	CTS0	GND
6	DTR0	RTS1	DCD0	CTS1
7	TxD0	GND	TxD1	GND
8	RxD0	RxD1	TxD2	TxD3
9	RXD2	GND	RxD3	GND
10	USB_HDMA	USB_HDPA	RxD5	TxD5
11	USB_HDMB	USB_HDPB	NC	GND
12	USB_DDM	USB_DDP	I2C_DATA	CAN1_TxD
13	I2C_CLK	GND	CAN1_RxD	GND
14	CAN_VCC	FPGA_IO44	FPGA_IO46	FPGA_IO45
15	FPGA_IO48	GND	FPGA_IO47	GND
16	FPGA_IO50	FPGA_IO49	FPGA_IO52	FPGA_IO51
17	FPGA_IO53	GND	FPGA_IO54	GND
18	FPGA_IO56	FPGA_IO55	FPGA_IO58	FPGA_IO57
19	FPGA_IO60	GND	FPGA_IO59	GND
20	FPGA_IO62	FPGA_IO61	FPGA_IO63	FPGA_IO64
21	FPGA_IO66	GND	FPGA_IO65	GND
22	FPGA_IO68	FPGA_IO67	FPGA_IO70	FPGA_IO69
23	FPGA_IO72	GND	FPGA_IO71	GND
24	FPGA_IO73	FPGA_IO74	FPGA_IO76	FPGA_IO75
25	FPGA_IO78	GND	FPGA_IO77	GND
26	FPGA_IO80	FPGA_IO79	VBAT	FPGA_IO81
27	NC	GND	NC	GND
28	NC	NC	NC	NC
29	NC	GND	NC	GND
30	3V3	NC	3V3	NC

Table 2: Pinout expansion connectors X200

X201	A	B	C	D
1	+2V5_EPHY	GND	GND	GND
2	GND	ETH_SPEED	GND	ETH_LINK/ACT
3	GND	GND	AD0	GND
4	ADTRG	AD1	ADVREF	AD2
5	SD_MCDA0	GND	SD_MCDB0	GND
6	SD_MCDA1	SD_MCDB1	SD_MCDA2	SD_MCDB2
7	SD_MCDA3	GND	SD_MCDB3	GND
8	SD_MCCK	SD_MCCDA	SD_MCCDB	SCK0
9	SCK1	GND	TIOA1	GND
10	SCK2	TIOB1	PCK1	TIOA2
11	RK0	GND	TIOB2	GND
12	TK0	TD0	RF0	RD0
13	TF0	GND	FPGA_IO0	GND
14	FPGA_IO1	FPGA_IO2	FPGA_IO3	FPGA_IO4
15	FPGA_IO5	GND	FPGA_IO6	GND
16	FPGA_IO7	FPGA_IO8	FPGA_IO9	FPGA_IO10
17	FPGA_IO11	GND	FPGA_IO12	GND
18	FPGA_IO13	FPGA_IO14	FPGA_IO15	FPGA_IO17
19	FPGA_IO16	GND	FPGA_IO18	GND
20	FPGA_IO19	FPGA_IO20	FPGA_IO21	FPGA_IO22
21	FPGA_IO23	GND	FPGA_IO24	GND
22	FPGA_IO25	FPGA_IO26	FPGA_IO27	FPGA_IO28
23	FPGA_IO29	GND	FPGA_IO30	GND
24	FPGA_IO31	FPGA_IO32	FPGA_IO33	FPGA_IO34
25	FPGA_IO35	GND	FPGA_IO36	GND
26	FPGA_IO37	FPGA_IO38	FPGA_IO39	FPGA_IO40
27	FPGA_IO41	GND	FPGA_IO42	GND
28	FPGA_IO43	NC	NC	NC
29	NC	GND	NC	GND
30	3V3	NC	3V3	NC

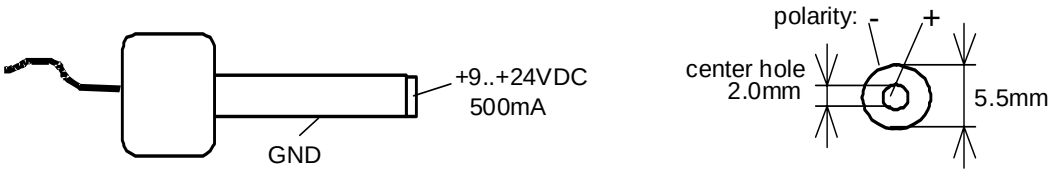
Table 3: Pinout expansion connectors X201

4 Component Descriptions

4.1 Power Supply

The Development Board needs a power supply of 9VDC to 28VDC unregulated. Power should be 12W minimum to supply the module and any peripheral circuits.

External power supply can be connected via Low Voltage Socket X600 or Terminal Block X601.



Please ensure that the correct polarity is applied to the terminal block. This is shown on the silkscreen on the PCB next to the terminal block.

From this voltage two switching regulators produce the onboard voltages (5VDC and 3,3VDC).
5VDC are only used for USB host. 3,3VDC supplies the ECUcore and all other peripheral elements.

4.2 ICE Interface

The ICE interface is for programming and debugging the 9G20-CPU. It's a pin contact stripes with standard contact spacing 2,54mm.

The connector layout is adjusted for using the ICE adapter from Amontec (www.amontec.com) with USB interface.

The following table shows the ICE/JTAG layout with pin names.

Signal	Pin	Pin	Signal
3V3	1	2	3V3
ARM_/NTRST	3	4	GND
ARM_TDI	5	6	GND
ARM_TMS	7	8	GND
ARM_TCK	9	10	GND
ARM_RTCK	11	12	GND
ARM_TDO	13	14	GND
/RESET	15	16	GND
not connected	17	18	GND
not connected	19	20	GND

Table 4: ICE/JTAG connector X403

If jumper JP503 is closed, signal /JTAGSEL on the ECUcore is set to high level and the Boundary Scan mode on the ECUcore-9G20 is active. Otherwise, if jumper JP503 is open, programming and debugging in ICE-mode is possible.

4.3 JTAG Interface

A separate JTAG interface is for programming the FPGA. With Jumper JP500, JP501 and JP502, it is possible to build a daisy chain with 9G20 and FPGA and accsess both via X502, e.g. for Boundary Scan. The connector is adjusted for the Boundary Scan System from Göpel (www.goepel.com), but the Lattice programming interface has a connector with discrete wires for each signal. For the JTAG mode only for FPGA, the following Jumper setting is necessary:

JP500	ARM_TCK FPGA_TCK	1-2 closed	JTAG-Signal FPGA_TCK is present on Pin 1 of X502
		3-4 closed	JTAG-Signal ARM_TCK is present on Pin 1 of X502
JP501	ARM_TMS	1-2 closed	JTAG-Signal FPGA_TMS is present on Pin 3 of X502

	FPGA_TMS	3-4 open	JTAG-Signal ARM_TMS is present on Pin 3 of X502
JP502	ARM_TDO FPGA_TDO ARM_TDI FPGA_TDI	1-2 closed	JTAG-Signal FPGA_TDI is present on Pin 7 of X502
		3-4 open	JTAG-Signal ARM_TDI is present on Pin 7 of X502
		5-6 closed	JTAG-Signal FPGA_TDO is present on Pin 5 of X502
		7-8 open	JTAG-Signal ARM_TDO is present on Pin 7 of X502

Signal	Pin	Pin	Signal
TCK	1	2	GND
TMS	3	4	GND
TDO	5	6	GND
TDI	7	8	GND
not connected	9	10	not connected

Table 5: JTAG connector X502

4.4 I/O Elements

The Development Board provides a lot of I/O elements for rapid development of software and for configuring and using the supplied software. Additional LEDs are directly connected to onboard periphery such as power supply and LAN and USB.

The next table shows the connection of each element at the µC.

element	connect to	IO on ECUcore
S400	3,3V	FPGA_IO73(Jumper), also FPGA_IO20, FPGA_IO0, FPGA_IO7
S401	3,3V	FPGA_IO74 (Jumper), also FPGA_IO21, FPGA_IO0, FPGA_IO7
S402	3,3V	FPGA_IO75 (Jumper), also FPGA_IO22, FPGA_IO0, FPGA_IO7
S403	3,3V	FPGA_IO76 (Jumper), also FPGA_IO23, FPGA_IO0, FPGA_IO7
D400	GND	FPGA_IO69
D401	GND	FPGA_IO70
D402	GND	FPGA_IO71
D403	GND	FPGA_IO72
D405 (LED RUN green)	3,3V	FPGA_IO77
D406 (LED ERROR red)	3,3V	FPGA_IO78
S404 (MRES)	GND	FPGA_IO79
S404 (STOP)	3,3V	FPGA_IO80
S404 (RUN)	3,3V	FPGA_IO81
D407 (/SHDN)	3,3V	/SHDN
D408 (/RESET)	3,3V	/RESET
S405 "RESET"	GND	/MR
S406 "BOOT"	GND	/BOOT
R429 (Potentiometer)	3,3V - GND	AD0, AD1,AD2
X304 LED green	3,3V	Eth0-PHY Speed
X304 LED yellow	3,3V	Eth0-PHY Link/Act
S407 (Dip Switch 1-8)	3,3V	FPGA_IO8, FPGA_IO9, FPGA_IO10, FPGA_IO11, FPGA_IO12, FPGA_IO13, FPGA_IO14, FPGA_IO15, FPGA_IO0, FPGA_IO7
J400 PCB-Version	3,3V	FPGA_IO16, FPGA_IO17, FPGA_IO18, FPGA_IO19, FPGA_IO0, FPGA_IO7

Table 6: IO elements connected to the ECUcore

LED	connect to	Function
D604 (yellow)	3,3V	3,3V-Supply
D605 (yellow)	5V	5V-Supply

Table 7: LEDs connected to onboard ICs

4.5 Ethernet

The 9G20-CPU has one build-in Ethernet-MAC. One Ethernet-PHY (KS8721BL) is on the ECUcore at Ethernet0. The Delevopment Board features a RJ45-ModularJack X304 for connecting LAN.

Pin	Function
1	TX+
2	TX-
3	RX+
4	TDCT
5	RDCT
6	RX-
7	not connected
8	GND
Shield	connected with PE on bor holes X308 and X309

Table 8: Pinout of RJ45-connectors

The PHY provides autonegotiation, so that a standard patch cable can be used, a cross-link cable is not necessary.

4.6 USB

4.6.1 USB host

For using USB sticks as memory extension or with additional interfaces (e.g. WLAN), 2 USB host controllers are built in the 9G20-CPU. It serves two USB-A connectors (X305A/B).

Connector power pins are directly provided by the Development Board power supply of 5VDC and not monitored. A current limitation is available by a 500mA fuse, but handle with care!
The supply provides approx. 1,5A. If the power supply of 5VDC drops down (LED D605 switched off), put off the stick and do not use it again!

4.6.2 USB device

The 9G20-CPU has build in an USB device interface. It serves one USB-B connector (X310). There is no power supply on pin 1 of the connector, so the Device interface cannot be detected by the Development Board.

4.7 SD Card

SD card socket X400 provides standard microSD cards. It is connected to the ECUcore via MCC-Bus.

Pin	ECUcore-Pin
DATA0	SD_MCDA0
DATA1	SD_MCDA1
DATA2	SD_MCDA2
DATA3	SD_MCDA3
CMD	SD_MCCDA
CLK	SD_MCCK
SLOT closed/open	SD_SLOT (AD2 by set Jumper JP405 1-2) closed = 0, open = 1

Table 9: SD card connection

4.8 EEPROM

The 8kiByte EEPROM (Atmel AT25160) can be used for saving the configuration or logging data. It will be accessed by the SPI-Bus that is integrated in the FPGA.

Pin	ECUcore-Pin
/CS	/SPI_CS1
SI	SPI_MTSR
SO	SPI_MRST
SCK	SPI_CLK
/HOLD	3,3V
/WP	GND protected, 3,3Vnot protected (status of J401)

Table 10: EEPROM connection

4.9 ADC

The 9G20-CPU has one build-in ADC with 3 analog inputs.
Some analog values can be adjusted by Potentiometer R429 and interpreted by software.

Pin	ECUcore-Pin
AD0	close jumper JP405 pin 7-8
AD1	close jumper JP405 pin 5-6
AD2	close jumper JP405 pin 3-4

Table 11: ADC connection

4.10 CAN

The 9G20-CPU has not build-in a CAN controller but a SPI controller on the ECUcore.
On the Development Board, there is a 5V- CAN transceiver (82C251TN3) and a male DSUB9 connector (X303).
The connector pinout is compatible to CANopen standard.

Pin	Function
4,5,8,9	not connected
1	close jumper JP303 5VDC CAN_VCC, open jumper JP303 not connected
2	CANL
3,6	GND
7	CANH
Shield	connected with PE on bor holes X306 and X307

Table 12: CAN connector pinout

CAN-bus can be terminated by 120R with Jumper JP302 (CAN0.

4.11 RS232

The Atmel 9G20 provides 5 UARTs. 3 of these 5 UARTs can be used as RS232 interface via DSUB connectors and 1 via a 3-pin-socket on the Development Board.

ECUcore-UART	Name on Devboard	connector	gender	communication signals
UART0	COM0	X300	female	RxD0, TxD0
UART1	COM1	X300	female	RxD1, TxD1
UART2	COM2	X302	socket	RxD2, TxD2
UARTD	COMD	X301	female	DRXD, DTXD

Table 13: RS232 connector pinout

All UARTs must be configured via jumper settings of JP300 and JP301. For communicating with the PC, an extension can be used (no null modem required).

RS232-Interface signal onECUcore	Connector	Jumper
TXD0, RXD0	X300	JP300 5-6, JP301 5-6
TXD1, RXD1	X300	JP300 7-8, JP301 7-8
DTXD, DRXD	X301	JP300 3-4, JP301 3-4
TXD2, RXD2	X302	JP300 1-2, JP301 1-2

Table 14: RS232 jumper settings

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